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Docket No.: 042390.P10571

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| In re Application of:<br>Blaise B. Fanning<br>Application No.: 09/823,126<br>Filed: March 30, 2001<br>For: PREFETCH CANCELING BASED ON MOST RECENT ACCESSES | Examiner: Gary J. Portka<br>Art Group: 2188 |



APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicant submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicant also submit herewith our check number 31271 in the amount of $440.00 to cover the cost of filing the opening brief as required by 37 C.F.R. § 1.17(f) and one-month extension fee. Please charge any additional fees or credit any overpayment to our deposit Account No. 02-2666. A duplicate copy of the Fee Transmittal is enclosed for this purpose.

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## I. REAL PARTY IN INTEREST

The real party in interest is the assignee, Intel Corporation.

## II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the appellants, the appellants' legal representative, or assignee, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

## III. STATUS OF CLAIMS

Claims 1-30 of the present application are pending and remain rejected. The Applicant hereby appeals the rejection of claims 1-30.

## IV. STATUS OF AMENDMENTS

The Applicant filed an amendment on January 16, 2004, in response to a Final Office Action issued by the Examiner on December 30, 2003. In response to the January 16, 2004 amendment, the Examiner issued an Advisory Action on February 10, 2004. The Applicant filed a Notice of Appeal from the Advisory Action issued by the Examiner on March 30, 2004.

## V. SUMMARY OF INVENTION

The invention is a technique to cancel a prefetch request by a processor. A computer system 100 includes a processor 110, a memory control hub (MCH) 130, and a system memory 140. The MCH 130 includes a prefetch circuit 135 to prefetch information from the system memory 140 based upon request patterns generated by the processor 110[1].

The prefetch circuit 135 includes a prefetcher 210 and a prefetch monitor circuit 220. The prefetcher 210 receives data and instruction requests from the processor 110. The information to be prefetched may include program code or data, or both[2]. The prefetcher 210 receives the prefetch information including the requests for required data and prefetch addresses generated by the processor 110. From this information, the

[1] Specification, page 4, lines 20-24; page 5, lines 20-22.

memory controller 130 first generates memory requests to satisfy the processor data or instruction requests. Subsequently, the prefetcher 210 generates an access request to the memory via the prefetch monitor circuit 220. The prefetcher 210 passes to the prefetch monitor circuit 220 the currently requested prefetch address to be sent to the memory 140. The prefetcher 210 can abort the prefetch if it receives a prefetch cancellation request from the prefetch monitor circuit 220[3].

The prefetch monitor circuit 220 receives the prefetch addresses generated by the prefetcher 210. If the prefetch monitor circuit 220 accepts the prefetch request, it allows the prefetch access and the prefetch information such as the current prefetch address to pass through to the memory 140 to carry out the prefetch operation. If the prefetch monitor circuit 220 rejects, cancels, or declines the prefetch request, it will assert a cancellation request to the prefetcher 210 so that the prefetcher 210 can abort the currently requested prefetch operation[4].

The prefetch monitor circuit 220 includes a storage circuit 310 and a prefetch canceler 320. The storage circuit 310 stores the most recent request addresses generated by the processor 110, or from the prefetcher 210. The storage circuit 310 retains a number of the most recent addresses, i.e., addresses of the last, or most recent, L pieces of data. The storage circuit 310 is a queue that stores first-in-first-out (FIFO) prefetch addresses. Alternatively, the storage circuit 310 may be implemented as a content addressable memory (CAM). A FIFO of size L essentially stores the most recent L prefetch or request addresses. One way to implement such a FIFO is to use a series of registers connected in cascade[5].

In one embodiment, the storage circuit 310 includes L registers $315_1$ to $315_L$ connected in series or cascaded. The L registers $315_1$ to $315_L$ essentially operates like a shift register having a width equal to the size of the prefetch address. The registers are clocked by a common clock signal generated from a write circuit 317. The write circuit 317 may include logic gates to decode the cancellation request and the prefetch and data requests from the processor 110. If the prefetch canceler 320 provides no cancellation request, indicating that the current prefetch address does not match to at least P of the stored prefetch addresses in the L registers $315_1$ to $315_L$, then the current prefetch address

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[2] Specification, page 5, lines 1-3.
[3] Specification, page 7, lines 8-17.
[4] Specification, page 7, lines 18-27; page 8, lines 1-3.

is written into the first register after the L registers $315_1$ to $315_L$ are shifted. Otherwise, writing and shifting of the L registers $315_1$ to $315_L$ is not performed. The outputs of the registers are fed to the prefetch canceler 320 for matching purpose[6].

The prefetch canceler 320 matches the currently requested prefetch, data or instruction, request address with the stored prefetch, data, or instruction request addresses from the storage circuit 310. The prefetch canceler 320 includes a matching circuit 330, a cancellation generator 340, and a gating circuit 350[7].

The matching circuit 330 matches a current prefetch address associated with the access request with the stored prefetch, data or instruction, request addresses from the storage circuit 310. The matching circuit 330 includes L comparators $335_1$ to $335_L$ corresponding to the L registers $315_1$ to $315_L$. Each of the L comparators $335_1$ to $335_L$ compares the current prefetch address with each output of the L registers $315_1$ to $315_L$. Each of the L comparators $335_1$ to $335_L$ generates a comparison result[8].

The cancellation generator 340 generates a cancellation request to the prefetcher 210 when the current prefetch address matches to at least or exactly P stored addresses, where P is a non-zero integer. The number P may be determined in advance or programmable. The cancellation generator 340 includes a comparator combiner 345 to combine the comparison results from the comparators. The combined comparison result corresponds to the cancellation request[9].

The gating circuit 350 gates the access request to the memory 140. If the cancellation request is asserted, indicating that the access request for the prefetch operation is canceled, the gating circuit 350 disables the access request. Otherwise, if the cancellation request is negated, indicating that the access request is accepted, the gating circuit 350 allows the access to proceed to the memory 140[10].

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[5] Specification, page 7-21.
[6] Specification, page 8, lines 22-26; page 9, lines 1-17.
[7] Specification, page 9, lines 18-27.
[8] Specification, page 10, lines 1-13.
[9] Specification, page 10, lines 17-27.
[10] Specification, page 11, lines 6-11.

## VI. ISSUES

The issues are:

(1) whether claims 1-5 and 11-15 are anticipated under 35 U.S.C. §102(b) over U.S. Patent No. 5,996,061 issued to Lopez-Aguado ("Lopez-Aguado"), and

(2) whether claims 6-10 and 16-30 are obvious under 35 U.S.C. §103(a) over Lopez-Aguado in view of U.S. Patent No. 6,134,633 issued to Jacobs ("Jacobs").

## VII. GROUPING OF CLAIMS

Applicant contends that the claims of the present invention form into two groups. Group 1 includes claims 1-5 and 11-15 and Group 2 includes claims 6-10 and 16-30.

## VIII. ARGUMENTS

### A. Claims 1-5 and 11-15 Are Not Anticipated By Lopez-Aguado.

Claims 1-5 and 11-15 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,996,061 issued to Lopez-Aguado ("Lopez-Aguado"). Applicant respectfully traverses the rejection and contends that a prima facie case of anticipation has not been established. To anticipate a claim, the reference must teach every element of a the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ 2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the...claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989).

Lopez-Aguado discloses a method for invalidating data identified by software compiler. A prefetch engine adds a stride to the physical address to derive a prefetch address (Lopez-Aguado, Col. 7, lines 18-19). The prefetched addresses are discarded if the derived prefetch address is already stored within the prefetch queue (Lopez-Aguado, Col. 7, lines 66-67; Col. 8, line 1).

Lopez-Aguado does not disclose, either expressly or inherently, (1) a storage circuit to store prefetch addresses corresponding to most recent access requests, (2) a canceler to

cancel an access request when the access request matches to at least P of the stored prefetch address, and (3) a gating circuit to disable the access request when the access request is canceled.

1) The Examiner has not met the burden of proof to show inherency of a gating circuit.

In the final Office Action dated December 30, 2003, the Examiner states that "[a]pplicant argue that a process that needs to be terminated based on the presence of a variable in storage does not inherently require a gating circuit. Examiner disagrees and suggests that Applicant is attempting to read limitations into the claim that do not exist; as stated previously a circuit which passes or does not pass a signal (to terminate) based upon a control input (based on the proper address), is required to achieve the termination of prefetching based upon an address being found in the queue." In the Advisory Action dated February 10, 2004, the Examiner maintained the rejections. Applicant respectfully disagrees.

Claims 1, 11, and 21 recite at least two elements: (1) the access request matches to at least P of the stored prefetch addresses, and (2) a gating circuit to disable the access request.

In the rejecting claims 1, 11, and 21 under 35 U.S.C. §102(b), the Examiner cited Lopez-Aguado and argued that a gating circuit is inherent to terminate prefetching based upon the determination that an address is in the prefetch queue. In disputing this conclusion, Applicant argues that even assuming that a process is terminated based on the presence of a variable in storage, this termination does not inherently require a gating circuit. The Examiner now states that Applicant is attempting to read limitations into the claim that do not exist.

The Examiner has a burden of proof to provide a rationale of inherency. The Examiner has not met that burden, because the Examiner has not shown how a termination of prefetching inherently requires a gating circuit. Applicant contends that the Examiner's inherency reasoning is flawed because it does not identify the signal to be gated and the output signal of the gating circuit, if indeed it is required. The Examiner must provide rationale or evidence tending to show inherency. MPEP 2112. The fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. In re Rijckaert, 9 F.3d 1531, 1534, 28 USPQ2d

1955, 1957 (Fed. Cir. 1993). Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.' " In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) "In relying upon the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original)

Here, the Examiner apparently misapplies the inherency concept. The fact that a gating circuit may be present in the prior art is not sufficient to establish inherency. The Examiner must show (not just merely state) that a termination of prefetching necessarily requires a gating circuit.

2) The prior art reference discloses a derived prefetch address, not a prefetch address.

In the final Office Action dated December 30, 2003, the Examiner states that "a derived prefetch address is a prefetch address". (Final Office Action, page 5, paragraph 14). If this is true, what is the reason to call it a "derived" prefetch address? In the Advisory Action dated February 10, 2004, the Examiner stated that "[t]he prefetch queue stores prefetch addresses; whether they are "derived" is immaterial to the claim language". Applicant respectfully disagrees. Lopez-Aguado discloses that the derived prefetch address is the sum of a stride and an extracted physical address (Lopez-Aguado, col. 7, lines 18-20). A 102(b) rejection requires that the prior art reference must show the identical invention in as complete detail as is contained in the claim. See, for example, Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ 2d 1913, 1920 (Fed. Cir. 1989). Here, the derived prefetch address is not the same as the prefetch address.

3) The prior art reference does not disclose matching with the most recent prefetch address(es).

In the final Office Action dated December 30, 2003, the Examiner states that "since it is determined if the derived prefetch address is already in the queue, it is determined if it matches at least P addresses in the queue." (Final Office Action, page 5, paragraph 14). In the Advisory Action dated February 10, 2004, the Examiner further stated that "[m]atching a prefetch address in the queue reads on matching at least P since P is a non-zero integer

and thus may be one". Applicant respectfully disagrees. First, as argued above, Lopez-Aguado merely discloses derived prefetch address, not prefetch address. Second, Lopez-Aguado does not disclose that the address in the queue represent the most recent access requests from a processor. Third, determining if the derived prefetch address is already in the queue is not, expressly or inherently, equivalent to matching at least P prefetch address in the queue.

Therefore, Applicant believes that independent claims 1, 11, 21 and their respective dependent claims are distinguishable over the cited prior art references.

### B. Claims 6-10 and 16-30 Are Not Obvious Under Lopez-Aguado In View of Jacobs.

Claims 6-10 and 16-30 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lopez-Aguado in view of U.S. Patent No. 6,134,633 issued to Jacobs ("Jacobs"). Applicant respectfully traverses the rejection and contends that the Examiner has not met the burden of establishing a prima facie case of obviousness. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. MPEP §2143, p. 2100-129 (8th Ed., Rev. 2, May 2004). Applicant contends that there is no suggestion or motivation to combine their teachings, and thus no prima facie case of obviousness has been established.

Jacobs discloses a prefetch management in cache memory. A prefetch memory supports discarding of prefetch addresses that are associated with operations executed by the processor such as by employing a fully associative prefetch memory when comparing addresses of cache access operations to the addresses held in the prefetch memory (Jacobs, Col. 7, lines 4-10).

Lopez-Aguado discloses a method for invalidating data identified by software compiler as discussed above.

Lopez-Aguado and Jacobs, taken alone or in any combination, does not disclose, suggest, or render obvious (1) a gating circuit to disable an access request to a memory

when the access request is canceled and (2) a plurality of comparators to compare the current prefetch address with each of the stored prefetch address. There is no motivation to combine Lopez-Aguado and Jacobs because neither of them addresses the problem of - gating the access request to disable the access request to a memory. There is no teaching or suggestion that a gating circuit or a plurality of comparators is present. Lopez-Aguado and Jacobs, read as a whole, does not suggest the desirability of gating the access request. Furthermore, Jacobs merely discloses using a fully associative prefetch memory when comparing the addresses of cache access operations, not comparing a current prefetch access request with each of the stored prefetch address.

## IX. CONCLUSION

The Examiner failed to establish a prima facie case of anticipation in rejecting claims 1-5 and 11-15. The Federal Circuit stated that to anticipate a claim, the reference must teach every element of the claim. Vergegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989). Lopez-Aguado does not disclose, either expressly or inherently, (1) a storage circuit to store prefetch addresses corresponding to most recent access requests, (2) a canceler to cancel an access request when the access request matches to at least P of the stored prefetch address, and (3) a gating circuit to disable the access request when the access request is canceled.

In addition, the Examiner failed to establish a prima facie case of obviousness and failed to show there is teaching, suggestion or motivation to combine the references in rejecting claims 6-10 and 16-30. "When determining the patentability of a claimed invention which combined two known elements, 'the question is whether there is something in the prior art as a whole suggest the desirability, and thus the obviousness, of making the combination.'" In re Beattie, Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1462, 221 USPQ (BNA) 481, 488 (Fed. Cir. 1984). To defeat patentability based on obviousness, the suggestion to make the new product having the claimed characteristics must come from the prior art, not from the hindsight knowledge of the invention. Interconnect Planning Corp. v. Feil, 744 F.2d 1132, 1143, 227 USPQ (BNA) 543, 551 (Fed. Cir. 1985). "To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or

implicitly suggest the claimed invention or the Examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references." Ex parte Clapp, 227 USPQ 972, 973. (Bd.Pat.App.&Inter. 1985).

In the present invention, Lopez-Aguado and Jacobs, taken alone or in combination, do not disclose, expressly or implicitly, suggest, or render obvious the above elements. In addition, the Examiner failed to present a convincing line of reasoning as to why a combination of Lopez-Aguado, and Jacobs is an obvious application of prefetch canceling based on most recent accesses.

As a result, none of the cited references discloses, explicitly or implicitly, suggests, or renders obvious the present invention as recited in claims 1-30.

Applicant respectfully requests that the Board enter a decision overturning the Examiner's rejection of all pending claims, and holding that the claims are neither anticipated or rendered obvious by the prior art.

Respectfully submitted,

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Dated: June 29, 2004

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## X. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. (previously presented) An apparatus comprising:

a storage circuit coupled to a prefetcher to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from a processor, the prefetcher generating an access request to a memory when requested by the processor; and

a canceler coupled to the storage circuit and the prefetcher to cancel the access request when the access request matches to at least P of the stored prefetch addresses, P being a non-zero integer, the canceler including a gating circuit to disable the access request to the memory when the access request is canceled.

2. (original) The apparatus of claim 1 wherein the storage circuit comprises:

a storage element to store the plurality of prefetch addresses from the most recent access requests by the processor, the storage element being one of a queue with a predetermined size and a content addressable memory (CAM).

3. (original) The apparatus of claim 2 wherein the queue comprises:

a plurality of registers cascaded to shift the prefetch addresses each time the processor generates an access request.

4. (original) The apparatus of claim 3 wherein the canceler comprises:

a matching circuit to match a current prefetch address associated with the access request with the stored prefetch addresses.

5. (original) The apparatus of claim 4 wherein the canceler further comprises:

a cancel generator coupled to the matching circuit to generate a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

6. (original) The apparatus of claim 4 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with each of the stored prefetch addresses.

7. (original) The apparatus of claim 4 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

8. (original) The apparatus of claim 7 wherein the cancel generator comprises:

a comparator combiner coupled to the comparators to combine the comparison results, the combined comparison results corresponding to the cancellation request.

9. (original) The apparatus of claim 2 wherein the canceler comprises:

a matching circuit having an argument register to store the current prefetch address for matching with entries of the CAM.

10. (original) The apparatus of claim 9 wherein the canceler further comprises:

a cancellation generator to generate a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.

11. (previously presented) A method comprising:

storing a plurality of prefetch addresses in a storage circuit, the plurality of prefetch addresses corresponding to most recent access requests from a processor, the prefetcher generating an access request to a memory when requested by the processor; and

canceling the access request when the access request matches to at least P of the stored prefetch addresses, P being a non-zero integer; and

disabling the access request to the memory by a gating circuit when the access request is canceled.

12. (original) The method of claim 11 wherein storing comprises:

storing the plurality of prefetch addresses in one of a queue with a predetermined size and a content addressable memory (CAM).

13. (original) The method of claim 12 wherein storing the plurality of prefetch addresses in the queue comprises:

storing the plurality of prefetch addresses in a plurality of registers cascaded to shift the prefetch addresses each time the processor generates a prefetch request.

14. (original) The method of claim 13 wherein canceling comprises:

matching a current prefetch address associated with the access request with the stored prefetch addresses.

15. (original) The method of claim 14 wherein canceling further comprises:

generating a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

16. (original) The method of claim 14 wherein matching comprises:

comparing the current prefetch address with each of the stored prefetch addresses.

17. (original) The method of claim 14 wherein matching comprises:

comparing the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

18. (original) The method of claim 17 wherein generating the cancellation request comprises:

combining the comparison results, the combined comparison results corresponding to the cancellation request.

19. (original) The method of claim 12 wherein canceling comprises:

storing the current prefetch address in an argument register for matching with entries of the CAM.

20. (original) The method of claim 9 wherein canceling further comprises:

generating a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.

21. (previously presented) A system comprising:

a processor to generate prefetch requests;

a memory to store data; and

a chipset coupled to the processor and the memory, the chipset comprising:

a prefetcher to generate an access request to the memory when requested by the processor;

a prefetch monitor circuit coupled to the prefetcher, the prefetch monitor circuit comprising:

a storage circuit coupled to the prefetcher to store a plurality of prefetch addresses, the plurality of prefetch addresses corresponding to most recent access requests from the processor; and

a canceler coupled to the storage circuit and the prefetcher to cancel the access request when the access request matches to at least P of the stored prefetch addresses, P being a non-zero integer, the canceler including a gating circuit to disable the access request to the memory when the access request is canceled.

22. (original) The system of claim 21 wherein the storage circuit comprises:

a storage element to store the plurality of prefetch addresses from the most recent access requests by the processor, the storage element being one of a queue with a predetermined size and a content addressable memory (CAM).

23. (original) The system of claim 22 wherein the queue comprises:

a plurality of registers cascaded to shift the prefetch addresses each time the processor generates an access request.

24. (original) The system of claim 23 wherein the canceler comprises:

a matching circuit to match a current prefetch address associated with the access request with the stored prefetch addresses.

25. (original) The system of claim 24 wherein the canceler further comprises:

a cancel generator coupled to the matching circuit to generate a cancellation request to the prefetcher when the current prefetch address matches to the at least P of the stored prefetch addresses.

26. (original) The system of claim 24 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with each of the stored prefetch addresses.

27. (original) The system of claim 24 wherein the matching circuit comprises:

a plurality of comparators to compare the current prefetch address with contents of the plurality of registers, the comparators generating comparison results.

28. (original) The system of claim 27 wherein the cancel generator comprises:

a comparator combiner coupled to the comparators to combine the comparison results, the combined comparison results corresponding to the cancellation request.

29. (original) The system of claim 22 wherein the canceler comprises:

a matching circuit having an argument register to store the current prefetch address for matching with entries of the CAM.

30. (original) The system of claim 29 wherein the canceler further comprises:

a cancellation generator to generate a match indicator when the current prefetch address matches at least P of the entries, the match indicator corresponding to the cancellation request.